In the Claims:

1-4. (cancelled)

5. (currently amended) A bipolar transistor as claimed in claim 21 ~~2, further comprising a shallow trench isolation~~, wherein said dielectric region includes a layer of silicon nitride extending between said shallow trench isolation and said slanted sidewall of said collector pedestal.

6. (currently amended) A bipolar transistor as claimed in claim 5 further comprising a dielectric spacer, wherein said raised extrinsic base is ~~self~~-aligned to said emitter and spaced from said emitter by said dielectric spacer.

7. (cancelled)

8. (currently amended) A bipolar transistor, comprising:

a collector including a frustum-shaped collector pedestal having an at least substantially planar upper surface, a lower surface, and a slanted sidewall extending between said upper surface and said lower surface, wherein said upper surface has an area substantially less than an area of said lower surface;

an intrinsic base overlying all of said area of said upper surface of said collector pedestal;

an emitter overlying said intrinsic base;

a raised extrinsic base conductively connected to said intrinsic base; and

a dielectric region extending along said slanted sidewall of said collector pedestal adjacent to said upper surface~~A bipolar transistor as claimed in claim 7~~, wherein a centerline of said emitter is ~~aligned to~~ in alignment with a centerline of said collector pedestal.

9. (currently amended) A bipolar transistor as claimed in claim 8, wherein each of said centerlines of said emitter and said collector pedestal ~~are~~ is aligned to a wall of ~~within~~ a single opening in a layered stack of materials.

10. (currently amended) A bipolar transistor as claimed in claim ~~1~~ 8, wherein said intrinsic base includes a layer of a single-crystal semiconductor which forms a heterojunction with at least one of said emitter and said collector pedestal.

11-20. (cancelled)

21. (new) A bipolar transistor as claimed in claim 9, further comprising a shallow trench isolation and a conductive collector contact via, said collector further including a first active area and a second active area disposed in a single-crystal semiconductor region, each of said first and second active areas having major surfaces extending in lateral directions defining a major surface of said semiconductor region, said first active area underlying said collector pedestal and said second active area being

separated in at least one of said lateral directions from said first active area by said shallow trench isolation, wherein said collector contact via overlies said second active area.